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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,897	07/10/2003	Amr Fahim	030288	4071
23696	7590	12/09/2005		EXAMINER
QUALCOMM, INC 5775 MOREHOUSE DR. SAN DIEGO, CA 92121			ZWEIZIG, JEFFERY SHAWN	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 12/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.	FAHIM, AMR	
10/617,897		
Examiner	Art Unit	
Jeffrey S. Zweizig	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on 18 November 2005.  
2a) This action is **FINAL**.                    2b) This action is non-final.  
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 1,3-20,22-26 and 28 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) Claim(s) 15 is/are allowed.  
6) Claim(s) 1,3-20,22-26 and 28 is/are rejected.  
7) Claim(s) \_\_\_\_\_ is/are objected to.  
8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.  
10) The drawing(s) filed on 18 November 2005 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All    b) Some \* c) None of:  
1. Certified copies of the priority documents have been received.  
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) Notice of References Cited (PTO-892)  
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) Notice of Informal Patent Application (PTO-152)  
6) Other: \_\_\_\_\_.

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3-8, 10, 11 and 16-20, 22-26 and 28 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Feldtkeller (6,049,201).

Note that although the Feldtkeller reference was used for these rejections, the Milanesi et al. reference (6,040,736) appears to be equally applicable.

Fig. 1 discloses an NFET headswitch T coupled between a power supply and a load and a charge pump LP with a charge pump control signal VCO as recited in claim 1 and operating as recited in claims 3-6. Feldtkeller does not specify an FET load circuit as recited in claim 1, however, the load circuit is described as a motor vehicle electronic unit. Motor vehicle electronic units are known to include microprocessor systems which inherently include FET devices and typically require supply regulation. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the circuit of Fig. 1 with an load circuit comprising at least one FET device for the benefit of providing the load circuit with a regulated supply voltage.

Claims 1 and 3-6 are obvious.

Claims 7 and 8 are given little weight since they define no specific parameters.

Claims 7 and 8 recite general relationships that are inherent to the disclosed circuit configuration.

Further disclosed is an op amp RV as recited in claim 10 and functioning as recited in claim 11.

As pointed out above, Fig. 1 is disclosed as useful for motor vehicle electronics, which includes microprocessors, digital signal processors, memory units and analog circuits as recited in claims 16, 17, 18 and 19. Alternately, all of these applications typically require regulated supply voltages. Thus it would have been obvious to one of ordinary skill at the art at the time of the invention to apply Fig. 1 to microprocessors, digital signal processors, memory units and analog circuits for the benefit of providing a regulated supply voltage to the microprocessors, digital signal processors, memory units and analog circuits. Claims 16, 17, 18 and 19 are obvious.

Claims 20 and 22 are obvious for the reasons above.

As pointed out above, memory units (including SRAM) typically require regulated supply voltages. Thus it would have been obvious to one of ordinary skill at the art at the time of the invention to apply Fig. 1 to SRAM circuits for the benefit of providing a regulated supply voltage to the SRAM circuits. Claim 23 is obvious.

Claim 24 is obvious for the reasons above.

CMOS technology of .13 um or smaller is a known, common technology. It would have been obvious to one of ordinary skill in the art at the time of the invention to

implement Examiner's combination with such technology for the benefit of miniaturizing the circuit. As best understood, claim 25 is obvious.

Claim 26 is obvious for the reasons above.

Communication systems (including CDMA systems) typically require regulated supply voltages. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to apply Fig. 1 to CDMA systems for the benefit of providing a regulated supply voltage to the CDMA systems. Claim 28 is obvious.

3. Claim 9 remains rejected under 35 U.S.C. 103(a) as being unpatentable over Feldtkeller in view of Perelle et al. (6,295,189).

Feldtkeller does not appear to disclose a plurality of NFET devices as recited in claim 9. It is generally known that circuit components may be duplicated for the benefit of increasing desirable circuit parameters. It is specifically known that duplicate parallel transistors may be implemented for the benefit of out performing a lone transistor.

Perelle et al. Fig. 1, for example, discloses such a circuit 12m that out performs a lone transistor 12. It would have been obvious to one of ordinary skill in the art at the time of the invention to replace NFET head switch T with a plurality of parallel head switches for the benefit of decreasing the ON resistance of the headswitch, increasing power delivered to the load and reducing power dissipated by the headswitch. Claim 9 is obvious.

4. Claim 12-14 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Feldtkeller in view of Flock (5,977,743).

Feldtkeller does not appear to disclose the ADC elements recited in claims 12-14. Flock Fig. 1 discloses a headswitch circuit including an NFET T1 with a charge pump boosted gate control analogous to Feldtkeller. Flock further discloses a charge pump GVS, an ADC MS/AD1 and a controller SS/ES all coupled together and forming a regulating feedback system as recited in claim 12. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement this feedback system into Feldtkeller as taught by Flock for the benefit of exerting digital control over circuit regulation. Claim 12 is obvious.

The combination functions as recited in claim 13. Furthermore, the recited digital target value is provided by SS and/or SE and/or SA.

The target value is programmable by way of SS and/or SE and/or SA as recited in claim 14.

#### ***Response to Arguments***

5. Clearly signal VCO shown in Fig. 1 of the Feldtkeller reference is the claimed charge pump control signal for selectively enabling the charge pump to varying degrees based on the output of op amp RV such that the operation of the headswitch T is based at least in part on the pump control signal.

#### ***Conclusion***

6. Amended claim 15 appears to be allowable over the Prior Art of record.
  
7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey S. Zweizig whose telephone number is (571) 272-1758. The examiner can normally be reached on Monday thru Wednesday 6:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

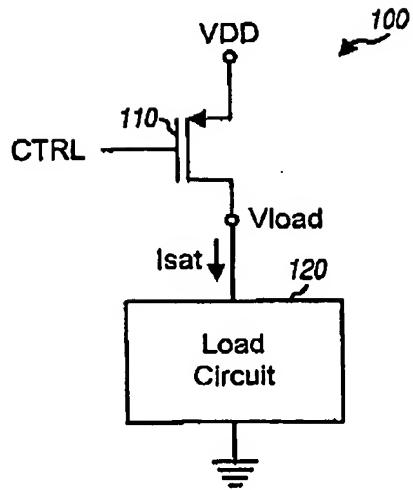


Jeffrey S. Zweizig  
Primary Examiner  
Art Unit 2816

JZ

Replacement Sheet  
030288

1

FIG. 1  
(Prior Art)

Approved  
JZ  
12/1/05

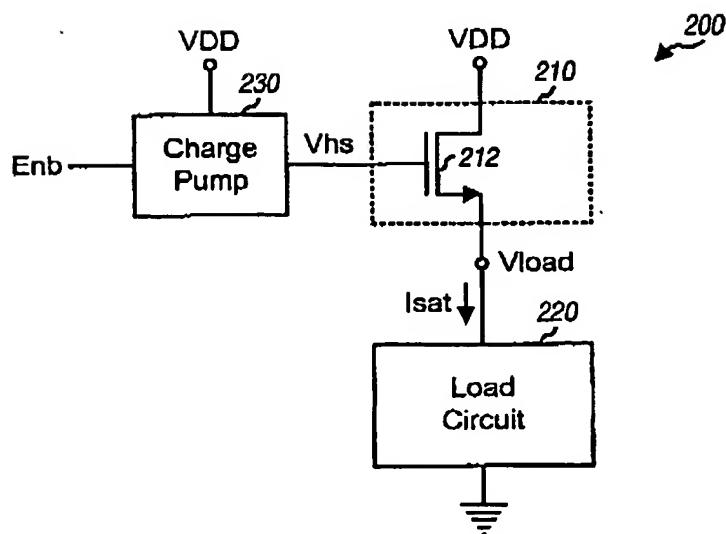


FIG. 2